

REMARKS

In the Office Action dated May 22, 2003 of the parent application (Application No. 10/184,486; filed June 28, 2002) of the instant continuation application, claims 1-5, 11, 15, 18, and 22 of the parent application were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,177,989 to Bruce (hereinafter "the *Bruce* reference"). Additionally, claims 1, 9-11, 16-18, and 23-24 of the parent application were rejected under 35 U.S.C. §102(b) as being anticipated U.S. Patent No. 5,189,365 to by Ikeda et al. (hereinafter "the *Ikeda* reference").

In the present Preliminary Amendment, Applicant seeks to place claims 1-15 of the instant application in condition for allowance by distinguishing these claims from the *Bruce* and *Ikeda* references. Claims 1-15 are currently pending, of which claims 1, 8, and 12 are in independent form. Favorable consideration of the present application as currently constituted is respectfully requested.

Regarding the Bruce reference

In the above-mentioned Office Action, the Examiner commented as follows in applying the *Bruce* reference with respect to the §102(b) rejection:

As to claims 1, 5, 11, 15, 18, 22, Bruce discloses in Fig. 2, 3, a system comprising: a device under test (DUT 200) assembly including said IC, wherein the IC includes at least one node (see figure 2) operable to be stimulated to a stuck-at fault condition by a certain frequency of electromagnetic (EM) radiation (via 252); a probe operable (beam 270, 274) with a laser voltage probe to stimulate the DUT assembly with said frequency of EM radiation; and a test pattern generator (generate the test vectors not shown, see col. 3, lines 25-45) and interface system (inherent) interfacing with the DUT assembly (200), the test pattern generator and interface system operating to apply a test vector to the DUT assembly (col. 3, lines 25-45), means (via detector 260) for comparing the IC's output against expected results associated with the test vectors set; and receive a corresponding response indicative of a fault coverage (via 264).

As claims 2-4, it appears that the IC is disposed on a package, die, or wafer.

The present invention, as defined by claim 1, is directed to a system for measuring fault coverage in an IC that includes a probe operable to stimulate at least one node of the IC to a stuck-at fault condition with a certain frequency of electromagnetic radiation. Applicant respectfully submits that the *Bruce* reference does not disclose Applicant's invention as recited in claim 1.

The *Bruce* reference teaches a system that utilizes laser induced current for semiconductor defect detection. In

particular, the *Bruce* reference employs a laser source to generate electromagnetic radiation for detecting short circuits that are already present in a semiconductor device. Applicant's invention, on the other hand, discloses a fault coverage measurement system having a probe that is operable to stimulate node to a stuck-at fault condition with electromagnetic radiation. That is, as will be shown below, the system of the *Bruce* reference detects short circuits in an IC rather than induce stuck-at fault conditions at one or more locations in the IC for coverage measurement.

With reference to FIG. 2 of the *Bruce* reference, a beam 202 of laser light illuminates nodes 204 of a semiconductor structure 200. If a node has a short circuit, a current is induced therein, thereby causing a photo-emission 206 which may be detected by a photo-emission detector 260 in order to produce an image of the integrated circuit 200. The *Bruce* reference describes the detection process as follows:

FIG. 2 is a perspective view of a semiconductor structure 200 at which a beam 202 of laser light is directed. The dashed line block 204 is an exaggerated depiction of a node within the integrated circuit. The beam 202 of laser light, also exaggerated in size, illuminates node 204. If the node has a short circuit, a current is induced therein, thereby causing a photo-emission 206. While not shown, it will be appreciated that some portion of the laser light 202 is also reflected from the integrated circuit 200. It is expected that the photo-emission will have a wavelength of 0.9 to 2 μm for flip chips and will have an intensity that is greatest at about 1.3 μm .

The coordinates of the photo-emission 206 can be mapped to a region of the integrated circuit 200 in order to ascertain the particular circuitry that comprises the node 204. Once the node has been identified, various test vectors can be constructed and applied to exercise the particular circuitry to confirm the defect.

The invention finds use in inspection of both conventional integrated circuit devices, for example, those having the front side exposed, and in flip-chip devices. For conventional devices, the invention can be used to quickly identify the location of a potential defect by scanning the front side of the integrated circuit. The invention is particularly useful for inspecting flip-chip integrated circuits because in such a circuit the front side is obscured from view. Therefore, conventional techniques for visual inspection of the front side of a flip-chip integrated circuit are difficult, if not impossible without destroying the circuit. Column 3, line 45 - column 4, line 6.

Hence, the *Bruce* reference is concerned with employing electromagnetic radiation to detect short circuits in order to inspect and map semiconductor structures. The *Bruce* reference is not concerned with employing electromagnetic radiation to stimulate stuck-at faults in order to measure fault coverage. Further, the *Bruce* reference neither discloses nor suggests a system for measuring fault coverage in an IC that includes a probe operable to stimulate at least one node of the IC to a stuck-at fault condition with a certain frequency of electromagnetic radiation as recited by Applicant in claim 1. Accordingly, Applicant respectfully submits that claim 1 is patentable over the *Bruce* reference.

Claims 2-7 depend from base claim 1 and add further limitations thereto. Therefore, it is respectfully submitted that claims 2-7 are also patentable over the *Bruce* reference.

With respect to base claim 8, the present invention is directed to a method for measuring fault coverage in an integrated circuit. Similar to claim 1, claim 8 includes limitations directed to employing a probe for stimulating at least one node of the IC to a stuck-at fault condition with a certain frequency of electromagnetic radiation. Accordingly, in view of the foregoing remarks, Applicant respectfully submits that claim 8 is patentable over the *Bruce* reference.

Claims 9-11 depend from base claim 8 and add further limitations thereto. Accordingly, Applicant respectfully submits that dependent claims 9-11 are also patentable over the *Bruce* reference.

With respect to base claim 12, the present invention is directed to a system for measuring fault coverage in an integrated circuit. Similar to claim 1, claim 12 includes limitations directed to employing a certain frequency of electromagnetic radiation to stimulate at least one node of the IC to a stuck-at fault condition. Accordingly, in view of the foregoing remarks, Applicant respectfully submits that base claim 12 and the claims depending therefrom, i.e., claims 13-15, are patentable over the *Bruce* reference.

Regarding the Ikeda reference

In the above-mentioned Office Action, the Examiner further commented as follows in making the §102(b) rejection:

As to claims 1, 11, 18, Ikeda et al. disclose in Fig. 2, Ikeda et al., disclose a method for measuring the fault coverage in an IC comprising the steps of: creating a stuck-at fault condition (col. 2, lines 10-12, and lines 48-50) at a select number of nodes associated with the IC; applying a test vector set (col. 2, lines 13-15 and lines 48-50) to the IC upon creating said stuck-at fault condition; comparing the IC's output against expected results associated with said test vector set (col. 2, lines 19-25 and lines 65-69); and determining fault coverage detected by the test vector set (col. 2, lines 20-25, and lines 65-69; col. 3, lines 1-6).

As to claims 9-10, 16-17, 23-24, Ikeda et al. disclose wherein the stuck-at fault condition comprising a stuck-at zero and stuck-at one condition (col. 2, lines 30-35).

As previously discussed, the present invention, as defined by the pending base claims 1, 8 and 12, includes the limitations directed to stimulating at least one node of an IC for creation thereat a stuck-at fault condition with a certain frequency of electromagnetic radiation. Applicant respectfully submits that the *Ikeda* reference does not disclose or even allude to the Applicant's invention as currently defined.

The *Ikeda* reference teaches a method of locating a fault in a logic IC device. In particular, the *Ikeda* reference discloses a method for gathering data from a logic IC device and using the gathered data to generate a test data file for performing a fault

simulation, wherein stable faults are introduced in logical operation data that serves as input data.

With reference to FIGS. 1 and 2 of the *Ikeda* reference, a logic IC device 20 having a fault is tested by an LSI laser 21 and the results of the test are stored in a test result file 3 which provides a fault location result 4 that includes information on coordinates, type and function of the faulty logic cell. Where a fault test condition is rendered unreliable due to a racing hazard or the like, a fault simulation may be performed by analyzing the fault location result 4 and using a faulty logic operation data file 5 which serves as input data for the fault simulation. Logic operation data contained in the faulty logic operation data file 5 includes simulated (i.e., virtual) stable faults or stuck-at faults at particular logic cells in order to avoid racing hazards. The actual results of the fault simulation may then be compared to the expected results to provide further information relative to locating the faults in the logic IC. The *Ikeda* reference describes this fault detection process as follows:

Referring now to FIGS. 1 and 2, a logic IC device 20 in which a fault has actually occurred is tested by an LSI tester 21, and a known AFL (Automatic Fault Location, refer, for example, to "1990 International Test Conference" pp. 860-870) is performed on the basis of its test result (for example, information on input and output values on respective pins of the tested device chip, the number and positions of faulty input and output pins and so on) recorded in a test

result file 3 to obtain a fault location result 4 which includes, for example, information on coordinates, type and function of a faulty logic cell, whether the fault has found on the output side or input side of the cell, and so on.

In the test result file 3, there are recorded logical states at respective input and output pins of a logic IC device, not shown, such as a logic LSI device and a logic VLSI device in a tri-state logic which represents logical states by "0", "1" and "X" (unknown).

Then, if there exists an ambiguous fault condition rendered undefinable due to a hazard or the like in the fault location result 4 obtained by producing an unknown output "X" due to hazard in data recorded in the test result file 3 and executing the AFL, one or more "stable" faults F, which are not influenced by hazard or the like, are intentionally produced in logical operation data which is to serve as input data for a fault simulation, later referred to, by a method shown, for example, in FIGS. 3 and 4, and logical operation data including the faults F is stored in a faulty logical operation data file 5. Column 3, line 42 - column 4, line 3.

Hence, the *Ikeda* reference discloses a method for locating a fault in a logic IC device that aims to avoid hazards caused by racing, by using virtual stable faults in a logic operation data file pertaining to the logic device. Applicant respectfully submits that the *Ikeda* reference neither discloses nor suggests the present invention's limitations directed to stimulating a node of an IC device to create thereat a stuck-at fault condition with electromagnetic radiation provided by a probe. Accordingly, Applicant respectfully submits that the present invention as

defined by the base claims 1, 8 and 12 is patentable over the *Ikeda* reference.

Further, the dependent claims 2-7, 9-11 and 13-15 that depend from the base claims 1, 8 and 12, respectively, introduce additional limitations therein. Consequently, it is believed that these dependent claims are also patentable over the *Ikeda* reference.

Based on the foregoing analysis, Applicant respectfully submits that the present patent application is in condition for allowance as it is believed that the currently claimed invention is patentable over the art applied in the May 22, 2003 Office Action of the parent application of the present patent application.

CONCLUSION

The Examiner is respectfully requested to consider the above-presented remarks prior to the substantive examination of the instant application. If there are any matters concerning this response that may be cleared up by telephone, please call Applicant's attorney at (972) 720-1202, ext. 228.

Respectfully submitted,



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